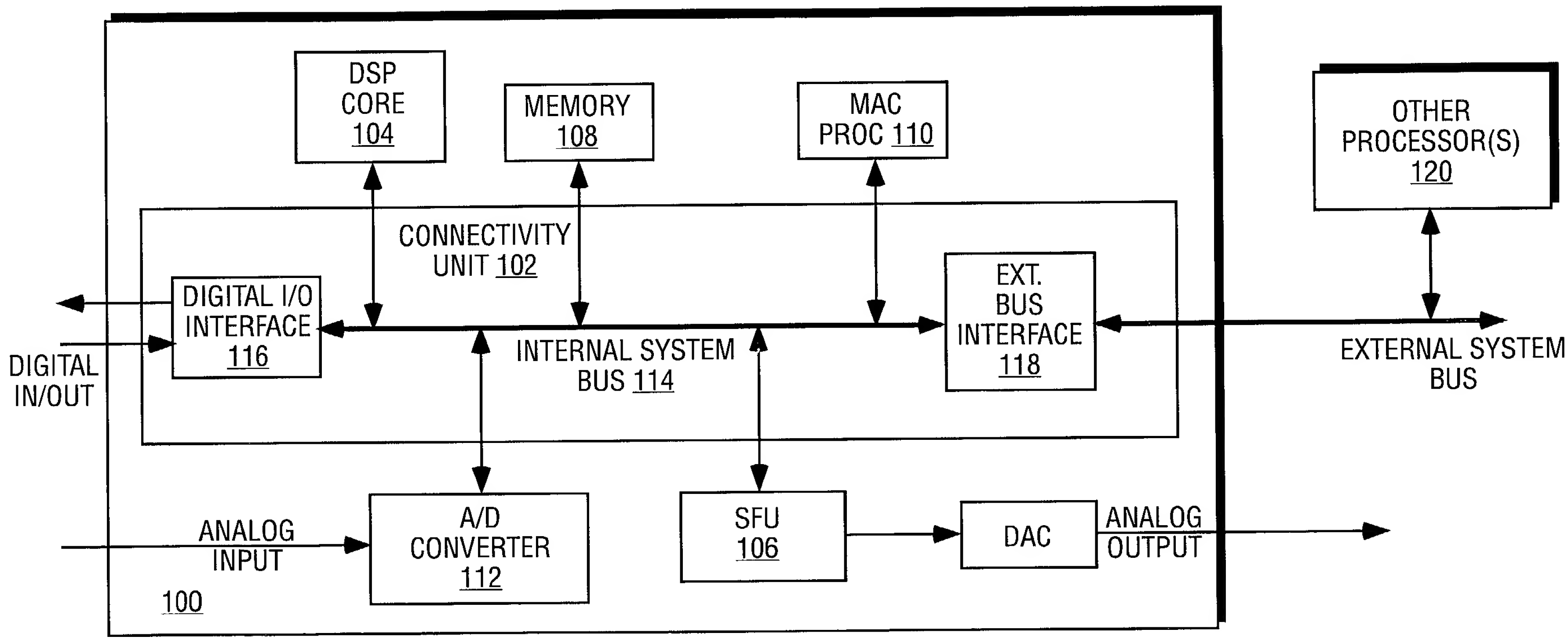
DSP
CORE
104
MEMORY
108
MAC
PROC 110
OTHER
PROCESSOR(S)
120
CONNECTIVITY
UNIT 102
DIGITAL I/O
INTERFACE
116
EXT.
BUS
INTERFACE
118
DIGITAL
IN/OUT
INTERNAL SYSTEM
BUS 114
EXTERNAL SYSTEM
BUS
ANALOG
INPUT
A/D
CONVERTER
112
SFU
106
DAC
ANALOG
OUTPUT
100

FIG. 1

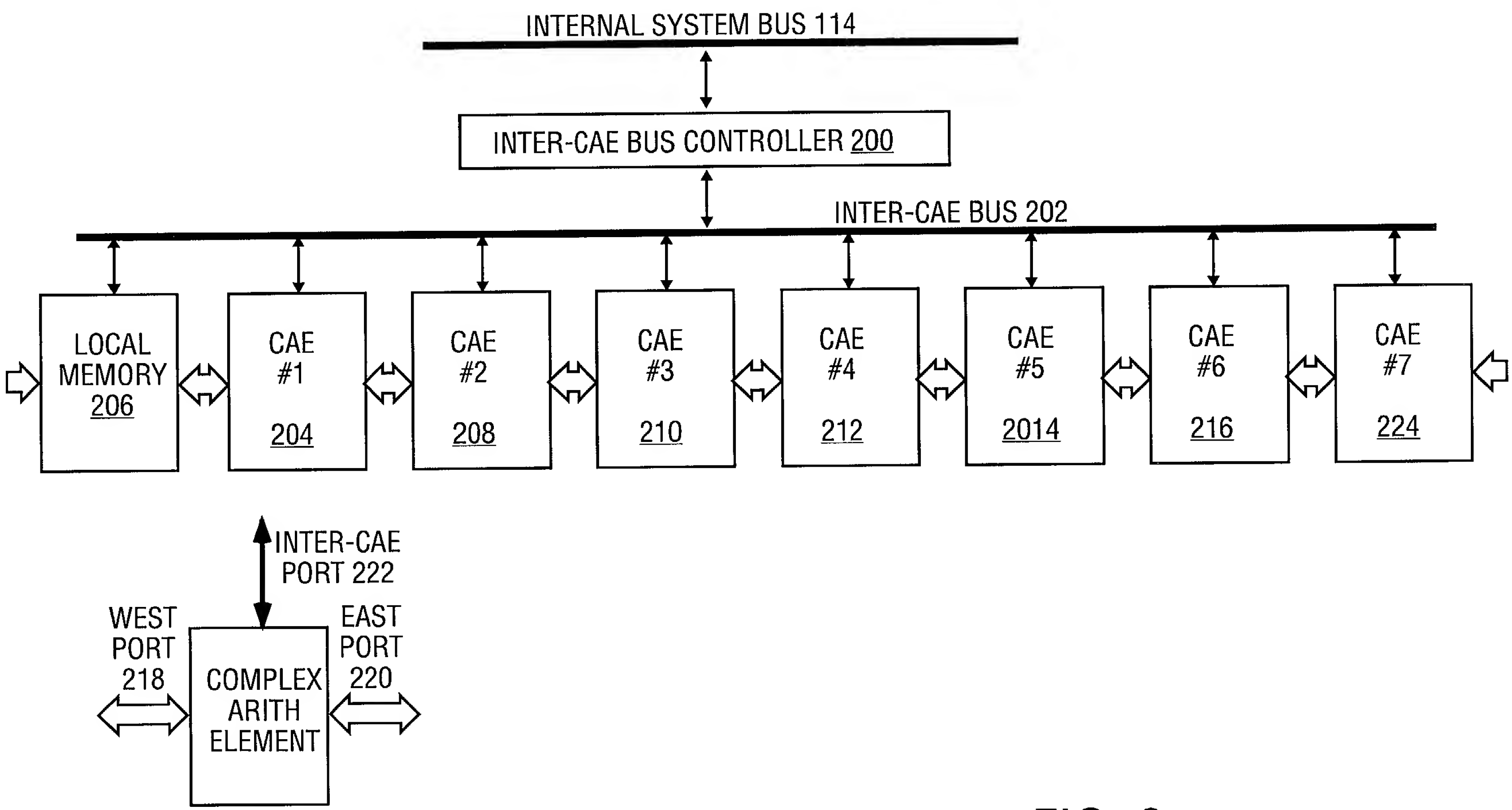
INTERNAL SYSTEM BUS 114
INTER-CAE BUS CONTROLLER 200
INTER-CAE BUS 202
LOCAL MEMORY 206
CAE #1 204
CAE #2 208
CAE #3 210
CAE #4 212
CAE #5 2014
CAE #6 216
CAE #7 224
INTER-CAE PORT 222
WEST PORT 218
COMPLEX ARITH ELEMENT
EAST PORT 220

FIG. 2

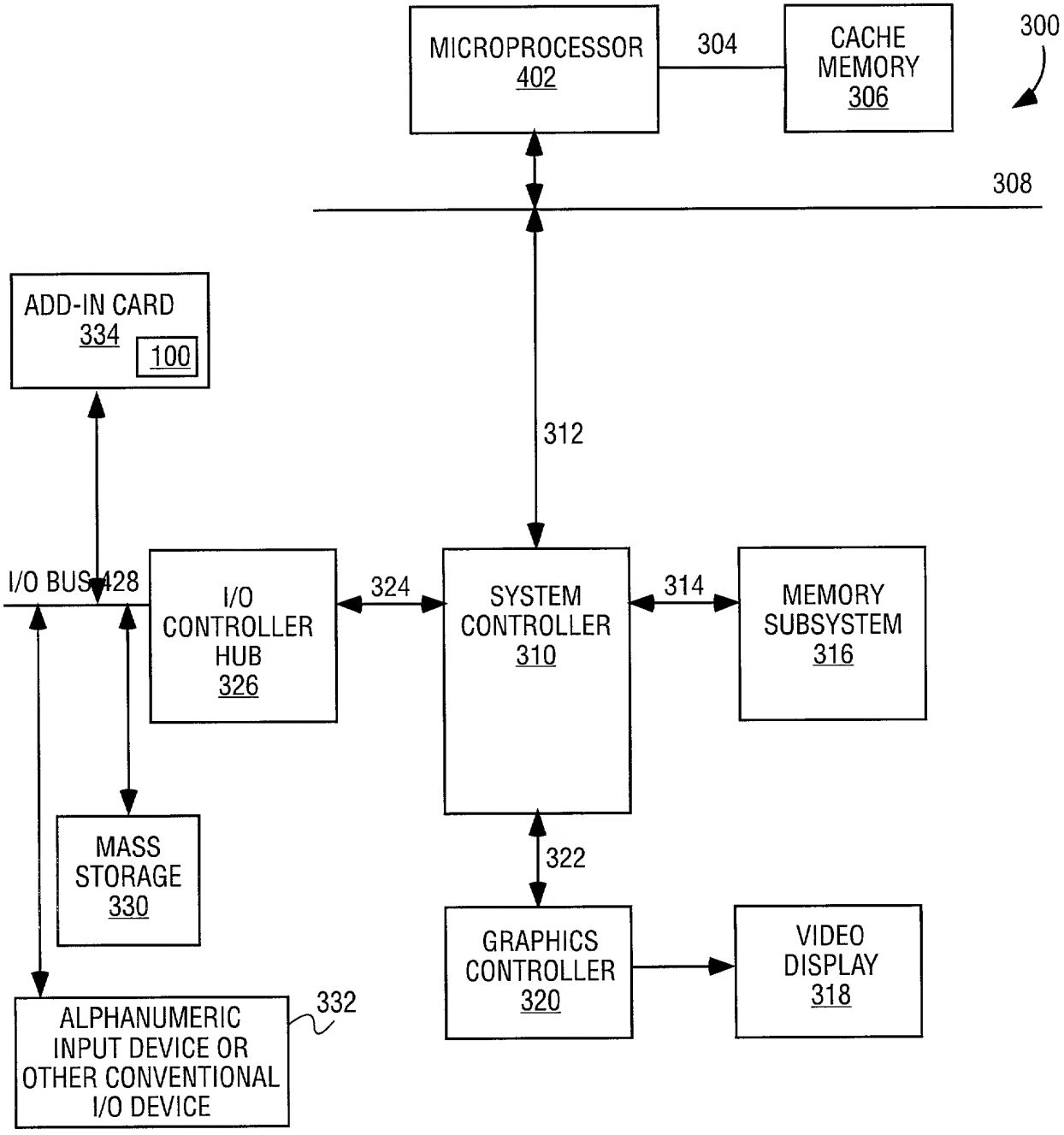
MICROPROCESSOR
402
304
CACHE
MEMORY
306
300
308
ADD-IN CARD
334
100
312
I/O BUS 428
I/O
CONTROLLER
HUB
326
324
SYSTEM
CONTROLLER
310
314
MEMORY
SUBSYSTEM
316
MASS
STORAGE
330
322
GRAPHICS
CONTROLLER
320
VIDEO
DISPLAY
318
ALPHANUMERIC
INPUT DEVICE OR
OTHER CONVENTIONAL
I/O DEVICE
332

FIG. 3

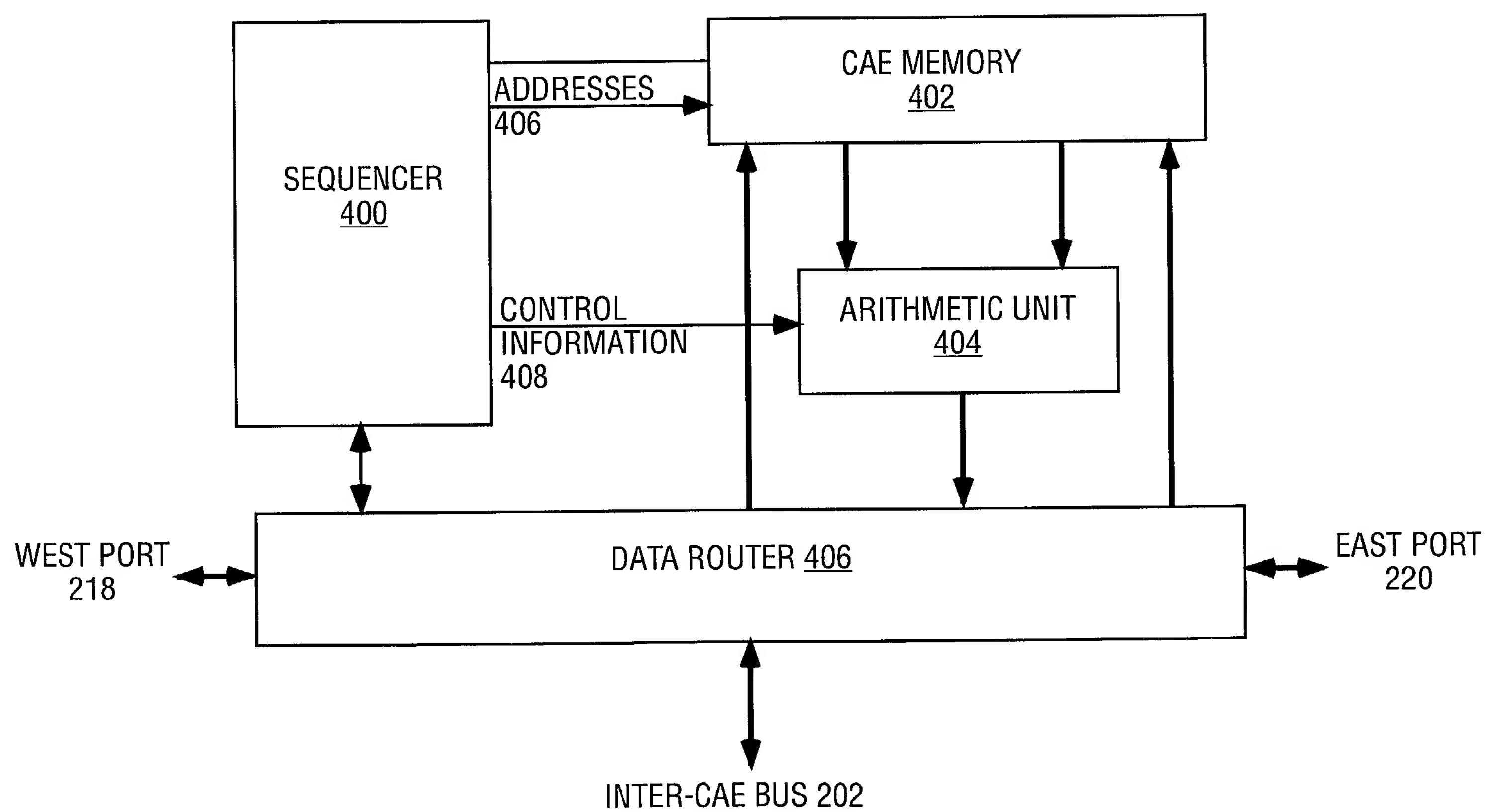
SEQUENCER
400
ADDRESSES
406
CONTROL
INFORMATION
408
CAE MEMORY
402
ARITHMETIC UNIT
404
DATA ROUTER 406
WEST PORT
218
EAST PORT
220
INTER-CAE BUS 202

FIG. 4

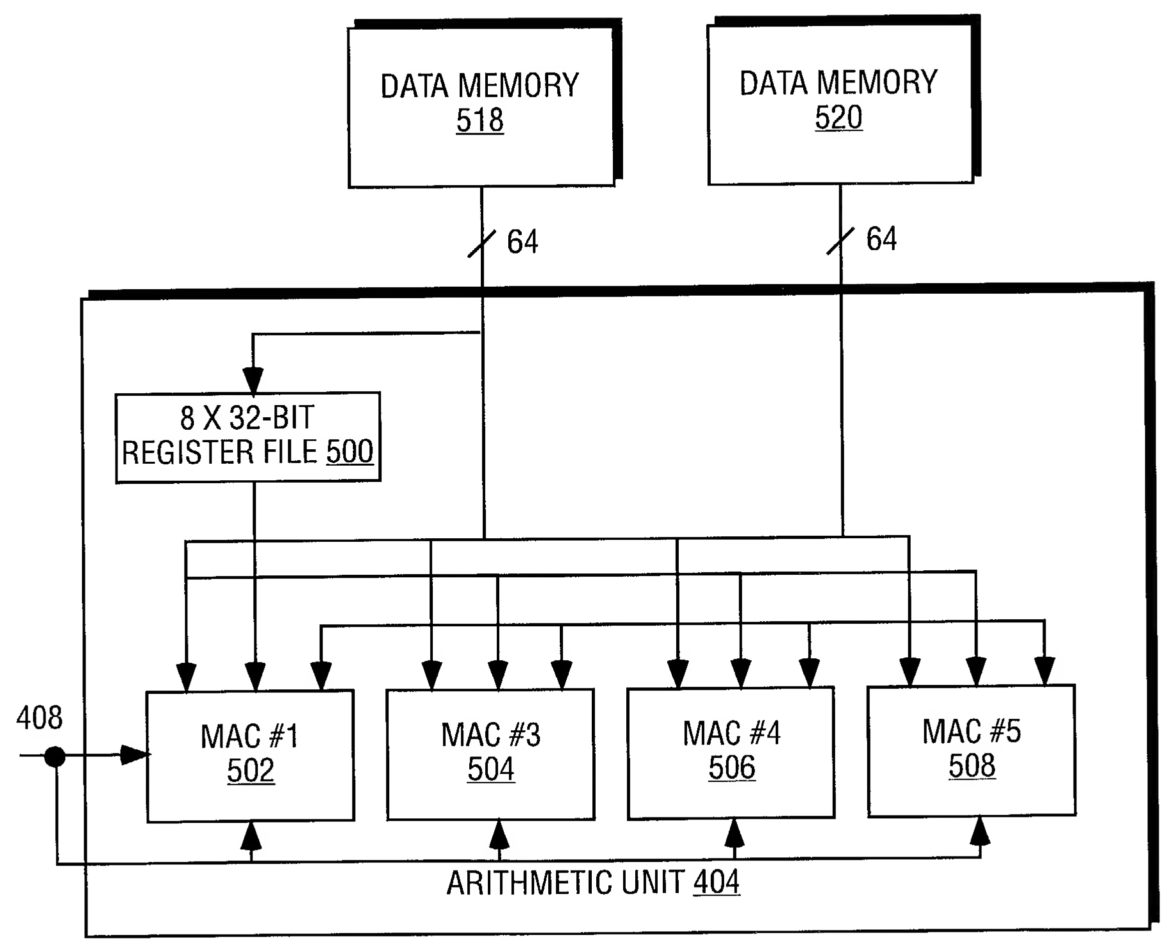

FIG. 5A

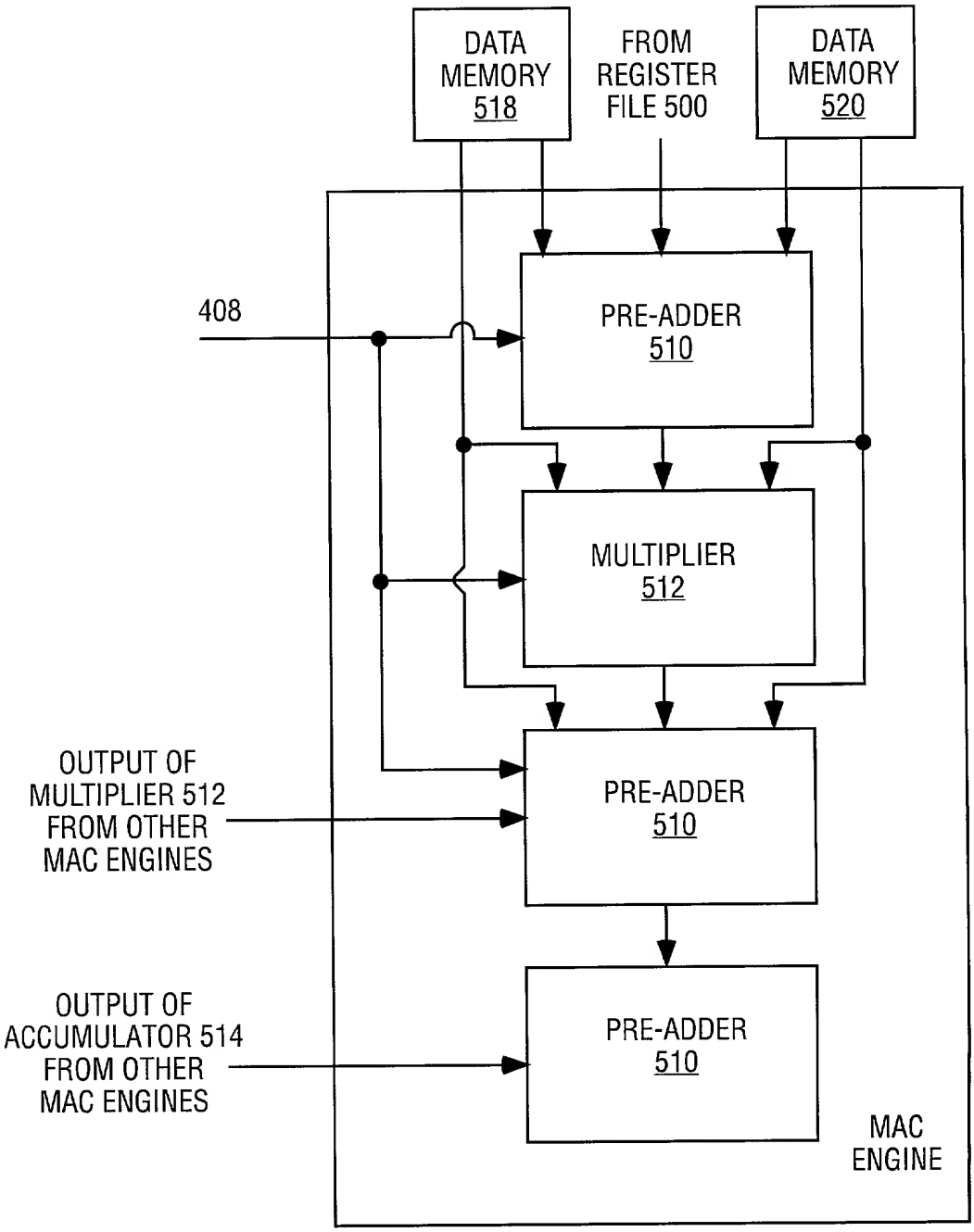
DATA MEMORY 518
FROM REGISTER FILE 500
DATA MEMORY 520
408
PRE-ADDER 510
MULTIPLIER 512
OUTPUT OF MULTIPLIER 512 FROM OTHER MAC ENGINES
PRE-ADDER 510
OUTPUT OF ACCUMULATOR 514 FROM OTHER MAC ENGINES
PRE-ADDER 510
MAC ENGINE

FIG. 5B

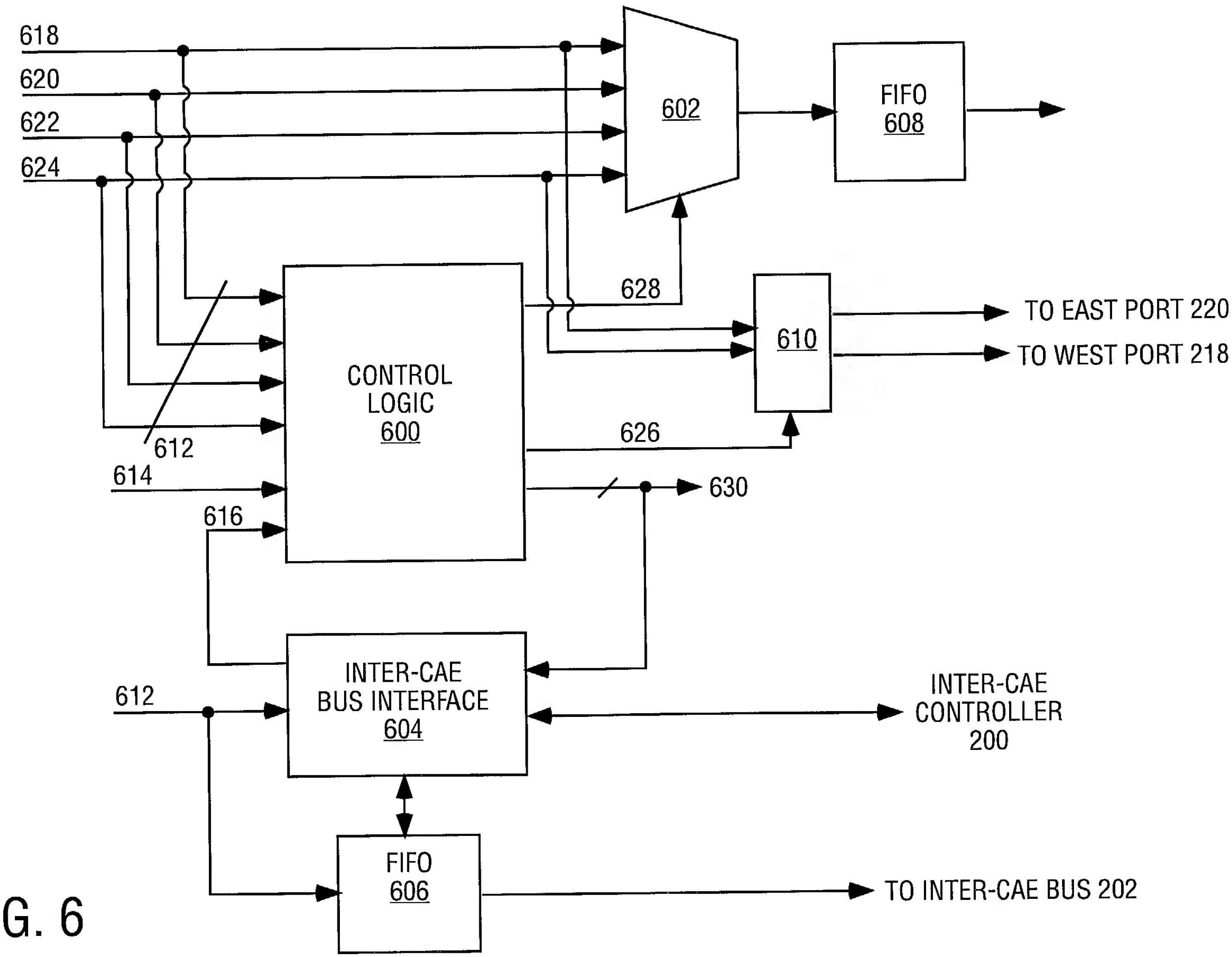
618
620
622
624
602
FIFO
608
CONTROL
LOGIC
600
612
614
616
628
610
TO EAST PORT 220
TO WEST PORT 218
626
630
INTER-CAE
BUS INTERFACE
604
612
INTER-CAE
CONTROLLER
200
FIFO
606
TO INTER-CAE BUS 202

FIG. 6